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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/516,082	03/01/2000	Satoshi Murakami	SEL163	3545

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EXAMINER

LEE, EUGENE

ART UNIT PAPER NUMBER

2815

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/516,082

Applicant(s)

MURAKAMI ET AL.

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 46-49, 52, 53, 56-79, 81 and 83-145 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 46-49, 52, 53, 56-79, 81 and 83-145 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Applicant's arguments, see Appeal Brief, filed 9/15/06, with respect to the rejection(s) of claim(s) 46-49, 52, 53, 56-79, 81, and 83-145 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

#### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 46 thru 49, 52, 53, 56 thru 79, 81, and 83 thru 145 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear how the color filter covers the entire first thin film transistor. In Fig. 28A, for example, color filter 2301 does not cover the entire n-channel TFT 701 because the pixel electrode 2307 creates a contact hole that prevents the color filter from covering the entire TFT.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Insofar as definite, claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140, and 144 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. 5,818,550 in view of Noda et al. 5,585,951. Kadota discloses (see, for example, FIG. 1) a semiconductor device comprising a first thin film transistor formed over a TFT substrate (insulating surface) 0 wherein the first thin film transistor comprises a semiconductor film 2, source and drain region S/D, channel forming region, gate insulating film, gate electrode 3; first inter-layer insulating film (interlayer insulating film) 4, electrodes (first conductive layer) 7, and pixel electrode 1. Kadota does not disclose a color filter, wherein the color filter covers the entire first thin film transistor. However, Noda discloses (see, for example, FIG. 18, and 19) a semiconductor device comprising a color filter 1803, which covers a thin film transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a color filter, wherein the color filter covers the entire first thin film transistor in order to have a flat color filter that is formed at one time that can evenly distribute light without defect.

Regarding the limitation "a semiconductor film comprising crystalline silicon", see, for example, column 3, line 64 wherein Kadota discloses the semiconductor film being a polycrystalline silicon thin film.

Regarding claim 139, see, for example, FIG. 1 wherein Kadota discloses a wired electrode (second conductive layer) 6.

6. Claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141, and 145 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109,

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110, 116, 139, 140, and 144 above, and further in view of Seo 6,323,521. Kadota in view of Noda does not disclose the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide. However, Seo discloses (see, for example, FIG. 6D) a semiconductor device comprising a gate insulating interlayer (interlayer insulating film) 219 over a thin film transistor. In column 9, lines 3-8, Seo discloses the gate insulating interlayer as being silicon oxide, silicon nitride or other suitable material. The gate insulating interlayer covers the thin film transistor and provides an adequate material for making contact holes. The contact holes are used to form contacts to source and drain regions of a thin film transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide for the interlayer insulating film in order to cover the thin film transistor and provides an adequate material for making contact holes, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 52, and 53, Kadota in view of Noda discloses (see, for example, FIG. 1 of Kadota) a semiconductor device comprising a thin film transistor formed over a TFT substrate (insulating surface) 0 wherein the thin film transistor comprises a semiconductor film 2, source and drain region S/D, channel forming region, gate insulating film, gate electrode 3; first inter-layer insulating film (first interlayer insulating film) 4, electrodes (conductive layer) 7, second inter-layer insulating film (passivation film) 5, color filter 9R/9G/9B, and pixel electrode 1. Kadota in view of Noda does not disclose the second inter-layer insulating film (passivation

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film) comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide. However, Seo discloses (see, for example, FIG. 6D) a semiconductor device comprising a passivation film (second interlayer insulating film) 231 over a thin film transistor. In column 10, lines 2-5, Seo discloses the passivation film as being silicon oxide or silicon nitride. The passivation film covers the source and drain electrodes of the thin film transistor and provides an adequate material for making contact holes. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide in order to cover the source and drain electrodes of the thin film transistor and provide an adequate material for making contact holes, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Claims 56, 62, 71, 74, 93, 103, 113, and 142 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140, and 144 above, and further in view of Ha 5,677,207. Kadota in view of Noda does not disclose LDD regions. However, Ha discloses (see, for example, FIG. 3G) a semiconductor device comprising LDD regions 38 in contact with a channel area 32a. In column 1, lines 48-63, Ha discloses that LDD areas reduce the electric field between the drain and channel area. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the LDD regions in order to reduce the electric field between the drain and channel area, and reduce leakage current.

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8. Claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, 115, and 143 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141, and 145 above, and further in view of Ha 5,677,207. Kadota in view of Noda in view of Seo does not disclose LDD regions. However, Ha discloses (see, for example, FIG. 3G) a semiconductor device comprising LDD regions 38 in contact with a channel area 32a. In column 1, lines 48-63, Ha discloses that LDD areas reduce the electric field between the drain and channel area. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the LDD regions in order to reduce the electric field between the drain and channel area, and reduce leakage current.

9. Claims 77, 78, and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140, and 144 above, and further in view of Matsumoto 5,323,042. Kadota in view of Noda does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary

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skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

10. Claims 79, 81, 87, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141, and 145 above, and further in view of Matsumoto 5,323,042. Kadota in view of Noda in view of Seo does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

11. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140, and 144 above, and further in view of Mikoshiba 5,499,123. Kadota in view of Noda discloses (see FIG. 1) a planarization film (resin film) 10. In column 5, lines 60-65, Kadota discloses the planarization film comprising an acrylic resin or polyimide resin used as an organic transparent material. Kadota in view of Noda does not disclose an electrode over the



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organic resin film; and an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween. However, Mikoshiba discloses (see, for example, FIG. 3B) a semiconductor device comprising a capacitance element 400 wherein the capacitance element comprises a shading layer (electrode) 312, insulating layer (oxide film) 314, and transparent layer (pixel electrode) 308. In column 4, lines 57-64, Mikoshiba discloses that a bias voltages can be applied to the capacitance element so that a brighter, clearer image can be attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include an electrode over the organic resin film; and an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with oxide film interposed therebetween in order to apply a bias voltage to an LCD device so that a brighter, clearer image may be attained.

12. Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141, and 145 above, and further in view of Mikoshiba 5,499,123. Kadota in view of Noda in view of Seo discloses a planarization film (resin film) 10. In column 5, lines 60-65, Kadota discloses (see FIG. 1) the planarization film comprising an acrylic resin or polyimide resin used as an organic transparent material. Kadota in view of Noda in view of Seo does not disclose an electrode over the organic

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resin film; and an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween. However, Mikoshiba discloses (see, for example, FIG. 3B) a semiconductor device comprising a capacitance element 400 wherein the capacitance element comprises a shading layer (electrode) 312, insulating layer (oxide film) 314, and transparent layer (pixel electrode) 308. In column 4, lines 57-64, Mikoshiba discloses that a bias voltage can be applied to the capacitance element so that a brighter, clearer image can be attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the electrode over the organic resin film; and an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with oxide film interposed therebetween in order to apply a bias voltage to an LCD device so that a brighter, clearer image may be attained.

13. Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Ha '207 as applied to claims 56, 62, 71, 74, 93, 103, 113, and 142 above, and further in view of Matsumoto 5,323,042. Kadota in view of Noda in view of Ha does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In

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column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

14. Claims 84 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 in view of Ha '207 as applied to claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, 115, and 143 above, and further in view of Matsumoto 5,323,042. Kadota in view of Noda in view of Seo in view of Ha does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

15. Claims 119, 120, and 126 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140, and 144 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Noda does not disclose one or more gate electrodes in addition to the gate

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electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

16. Claims 121, 122, 127, and 128 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141, and 145 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Noda in view of Seo does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

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17. Claim 123 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Ha '207 as applied to claims 56, 62, 71, 74, 93, 103, 113, and 142 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Noda in view of Ha does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

18. Claims 124, and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 in view of Ha '207 as applied to claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, 115, and 143 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Noda in view of Seo in view of Ha does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in

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addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

19. Claim 129, 130, and 136 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140, and 144 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Noda et al. '951 does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

20. Claim 131, 132, 137, and 138 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141, and 145 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Noda in view of Seo does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the

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time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

21. Claim 133 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Ha '207 as applied to claims 56, 62, 71, 74, 93, 103, 113, and 142 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Noda in view of Ha does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

22. Claim 134, and 135 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Noda et al. '951 in view of Seo '521 in view of Ha '207 as applied to claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, 115, and 143 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Noda in view of Seo in view of Ha does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the

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gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

***Response to Arguments***

23. Applicant's arguments with respect to claims 46-49, 52, 53, 56-79, 81, and 83-145 have been considered but are moot in view of the new ground(s) of rejection.

**INFORMATION ON HOW TO CONTACT THE USPTO**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

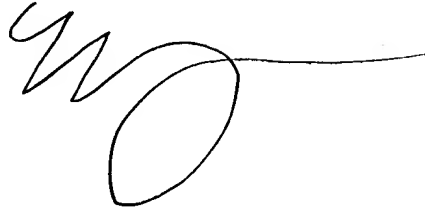


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Eugene Lee  
November 28, 2006

**EUGENE LEE**  
**PRIMARY EXAMINER**

A handwritten signature in black ink, consisting of a stylized 'E' followed by a large loop and a horizontal line extending to the right.